ADS8402/ADS8412EVM

User's Guide

December 2003

Data Acquistion

SLAU126

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±6 V and the output voltage range of 0 V and 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the ADS8402/ADS8412 16-bit, high speed, parallel interface analog-to-digital converter evaluation board. A complete circuit description as well as a schematic diagram and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- ❑ Chapter 1 – EVM Overview
- ❑ Chapter 2 – Analog Interface
- ❑ Chapter 3 – Digital Interface
- ❑ Chapter 4 – Power Supply Requirements
- ❑ Chapter 5 – Using the EVM
- ❑ Chapter 6 - ADS8402/ADS8412 BOM, Layout, and Schematic

Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com

Data Sheets:	**Literature Number:**
ADS8402	SLAS154
ADS8412	SLAS384
REF3040	SBVS032
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC1G04	SCLS318
THS4503	SLOS352

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

Figures

Tables

Chapter 1

EVM Overview

This chapter contains the features of the ADS8402/ADS8412.

Topic **Page**

1.1 Features

- Full-featured evaluation board for the high-speed ADS8402 (1.25 MSPS) and the ADS8412 (2 MSPS) high speed, 16-bit, single channel, parallel interface SAR-type analog-to-digital converters.
- Onboard signal conditioning
- Onboard reference
- Input and output digital buffer
- Onboard decoding for stacking multiple EVMs

1.2 Introduction

The ADS8402EVM and ADS8412EVM is a modular or stand alone EVM. It has the bare minimum circuitry to showcase the device under test and plug into prototype systems. The onboard decoding circuitry enables the user flexibility to map the A/D to different addresses in processor memory. The power, analog and digital control lines are on standard 0.1-in. header/socket connectors, at the edges of the PWB, making it easy to wire into prototype systems for evaluation. The EVM has been designed for direct evaluation of the analog-to-digital converter performance and operating characteristics. This EVM is compatible with the 5-6K interface board (SLAU104) from Texas Instruments and additional third party boards.

Chapter 2

Analog Interface

The ADS8402/ADS8412EVM analog-to-digital converter has a unipolar differential input. A unipolar differential input is a differential signal (inverting and noninverting input is 180 degrees out of phase) that is level shifted such that the signals levels are always equal to or above zero volts. The peak-to-peak amplitude on each input pin can be as large as the reference voltage. See the respective product data sheet for more information.

Topic **Page**

2.1 Signal Conditioning

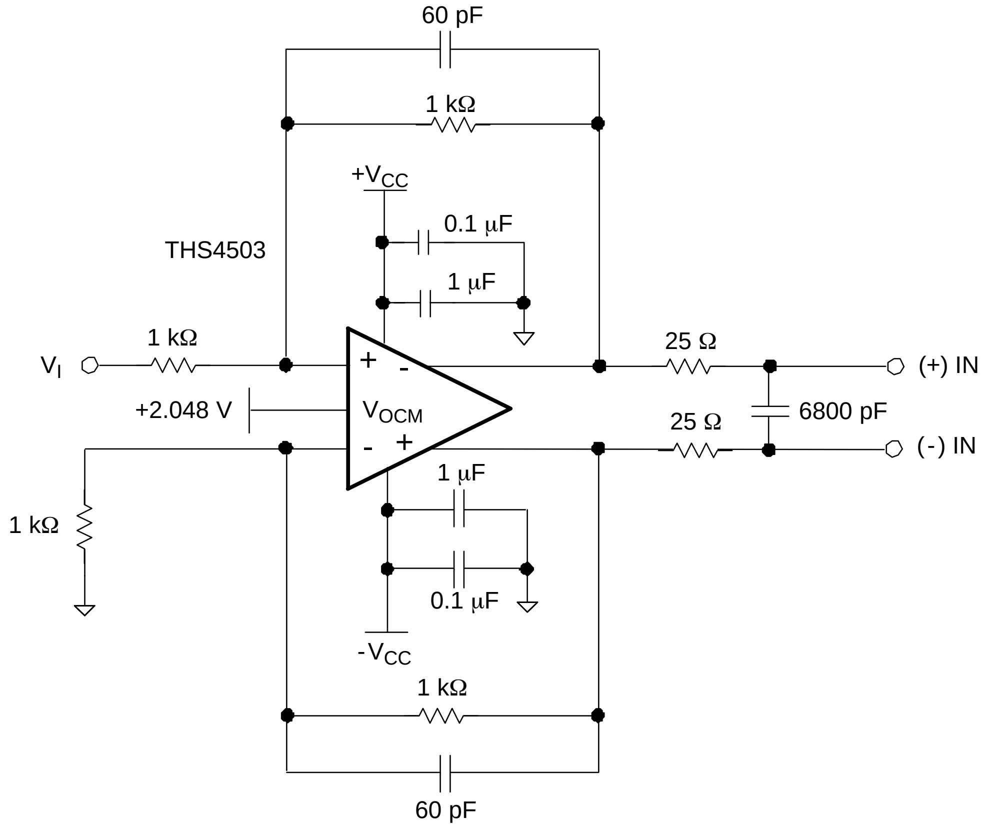
The ADS8402/ADS8412EVM comes installed with the unity gain buffer (U2) wired for single-ended in to differential out configuration. The common-mode voltage is derived from a REF3040 reference IC and is adjustable using a potentiometer (R9). The common-mode voltage pin of the THS4503 is set to 2 V on the evaluation module. A single-ended input signal can be applied at pin connector P1 or via SMA connectors J2 (noninverting input). The buffer circuit can be reconfigured for a unipolar differential input by installing resistor R6 and R8 and removing R1. The inverting leg of the differential signal should be applied to either connector P1 pin 1 or SMA connector J4 (inverting input). See Table 2-1 for the pinout of the analog connector, P1. See Chapter 6 for the EVM schematic.

Table 2-1. Analog Input Connector

Description	Signal Name	Connector.Pin#		Signal Name	Description
Inverting input	(-)	P1.1	P1.2	+	Noninverting input
Reserved	N/A	P1.3	P1.4	N/A	Reserved
Reserved	N/A	P1.5	P1.6	N/A	Reserved
Reserved	N/A	P1.7	P1.8	N/A	Reserved
Pin tied to ground	AGND	P1.9	P.10	N/A	Reserved
Pin tied to ground	AGND	P1.11	P1.12	N/A	Reserved
Reserved	N/A	P1.13	P1.14	N/A	Reserved
Pin tied to ground	AGND	P1.15	P1.16	N/A	Reserved
Pin tied to ground	AGND	P1.17	P1.18	N/A	Reserved
Reserved	N/A	P1.19	P1.20	REF+	External reference input

It is recommended the analog input to any SAR-type converter be buffered. The amplifier circuit in Figure 2-1 is the buffer circuit used on the ADS8402/ADS8412EVM. This circuit consists of the THS4503, a high-speed fully differential amplifier configured as a single-ended in to differential out, unity gain buffer. The circuit shown in Figure 2-1 was optimized to achieve the ac (i.e., SNR, THD, SFDR, etc.) specifications listed in the ADS8402 and ADS8412 data sheets. The 60-pF and 6800-pF capacitors in the signal path are polypropylene type, manufactured by the WIMA Corporation. Polypropylene capacitors cause the least distortion of the input signal.

Figure 2-1. Input Buffer Circuit



2.2 Reference

The EVM allows users to select from three reference sources. The ADS8402/ADS8412EVM provides an onboard 4.096-V reference, U3. The EVM also has the provision for users to supply a reference voltage via connecter P1 pin 20. The user reference voltage and onboard reference voltages can be filtered by installing amplifier U1. Both the ADS8402 and ADS8412 analog-to-digital converters have integrated onboard reference buffers; therefore, it is not necessary to buffer the voltage externally. The reference buffer circuit on the EVM is not populated with an amplifier. The EVM comes installed with an on-chip internal reference tied directly to the reference pin of the converter. See Chapter 6 for the schematic.

Table 2-2. Solder Short Jumper Setting

Reference Designator	Description	Jumper Setting	
		1-2	**2-3**
SJP1	Not used on the EVM		
SJP2	On-chip internal reference applied to reference pin	Installed†	
SJP3	Apply reference voltage from external source	Not Installed	Installed
	Apply voltage to amplifier, U2, common-mode voltage pin	Installed†	N/A
SJP4	Buffer onboard reference, REF3040	Installed	Not installed
	Buffer user reference voltage applied at P1 pin 20.	Not Installed	Installed
SJP5	Select REF3040 for reference voltage	Installed	Not installed
	Select buffered reference voltage	Not Installed	Installed

† Factory set condition

Chapter 3

Digital Interface

The ADS8402/ADS8412 EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient dual row header/socket combination at P2 and P3. Consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for a variety of mating connector options.

Table 3-1. Pinout for Parallel Control Connector P2

Connector.Pin	Signal	Description
P2.1	$\overline{\text{DC_CS}}$	Daughter card board select pin
P2.3		
P2.5		
P2.7	A0	Address line from processor
P2.9	A1	Address line from processor
P2.11	A2	Address line from processor
P2.13		
P2.15		
P2.17		
P2.19	$\overline{\text{INTc}}$	Set jumper W3 to select BUSY or inverted signal to be applied to this pin.

Note: All even numbered pins of P2 are tied to DGND.

The read ($\overline{\text{RD}}$), conversion start ($\overline{\text{CONVST}}$), and reset ($\overline{\text{RESET}}$) signals to the converter can be assigned to two different addresses in memory via jumper settings. This allows for the stacking of up to two ADS8402EVMs and/or ADS8412EVMs into processor memory. See Table 3-2 for jumper settings. Note, the evaluation module does not allow the chip select ($\overline{\text{CS}}$) line of the converter to be assigned to different memory locations. It is therefore suggested the $\overline{\text{CS}}$ line be grounded or wired to an appropriate signal of the processor.

Table 3-2. Jumper Settings for Decoder Outputs

Reference Designator	Description	Jumper Settings	
		1-2	**2-3**
W2	Set A[2..0] = 0x1 to generate $\overline{RD}$ pulse	Installed†	Not installed
	Set A[2..0] = 0x2 to generate $\overline{RD}$ pulse	Not installed	Installed
W5	Set A[2..0] = 0x3 to generate $\overline{CONVST}$ pulse	Installed†	Not installed
	Set A[2..0] = 0x4 to generate $\overline{CONVST}$ pulse	Not installed	Installed
W4	Set A[2..0] = 0x5 to generate $\overline{RESET}$ pulse	Installed†	Not installed
	Set A[2..0] = 0x6 to generate $\overline{RESET}$ pulse	Not installed	Installed

† Factory set condition

The data bus is available at connector P3, see Table 3-3 for pin out information.

Table 3-3. Data Bus Connector P3

Connector.Pin	Signal	Description
P3.1	D0	Buffered Data Bit 0 (LSB)
P3.3	D1	Buffered Data Bit 1
P3.5	D2	Buffered Data Bit 2
P3.7	D3	Buffered Data Bit 3
P3.9	D4	Buffered Data Bit 4
P3.11	D5	Buffered Data Bit 5
P3.13	D6	Buffered Data Bit 6
P3.15	D7	Buffered Data Bit 7
P3.17	D8	Buffered Data Bit 8
P3.19	D9	Buffered Data Bit 9
P3.21	D10	Buffered Data Bit 10
P3.23	D11	Buffered Data Bit 11
P3.25	D12	Buffered Data Bit 12
P3.27	D13	Buffered Data Bit 13
P3.29	D14	Buffered Data Bit 14
P3.31	D15	Buffered Data Bit 15

Note: All even numbered pins of P3 are tied to DGND.

This evaluation module provides direct access to all the analog-to-digital converter control signals via connector J3, see Table 3-4.

Table 3-4. Pinout for Converter Control Connector J3

Connector.Pin	Signal	Description
J3.1	$\overline{CS}$	Chip select pin. Active low
J3.3	$\overline{RD}$	Read pin. Active low
J3.5	$\overline{CONVST}$	Convert start pin. Active low
J3.7	BYTE	Byte mode pin. Used for 8-bit buses.
J3.9	$\overline{RESET}$	Reset pin. Active low.
J3.11	BUSY	Converter status output. High when a conversion is in progress.

Note: All even numbered pins of J3 are tied to DGND.

Chapter 4

Power Supply Requirements

The EVM accepts four power supplies.

- A dual ±Vs dc supply for the dual supply op-amps. Recommend ±7 Vdc supply.
- A single +5-Vdc supply for the analog section of the board (A/D + Reference).
- A single +5-V or +3.3-Vdc supply for the digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

1) Wire in the voltages at test points on the EVM. See Table 4-1.

Table 4-1. Power Supply Test Points

Test Point	Signal	Description
TP14	+BVDD	Apply +3.3 V or +5 V. See ADC data sheet for full range.
TP11	+AVCC	Apply +5 Vdc.
TP12	+VA	Apply +7 Vdc. Positive supply for amplifier.
TP13	-VA	Apply –7 Vdc. Negative supply for amplifier.

2) Use the power connector J1 and derive the voltages elsewhere. The pinout for this connector is shown in Table 4-2. If using this connector, set the W1 jumper to connect +3.3VD or +5VD from connector to +BVDD. Short between pins 1-2 to select +5VD or short between pins 2-3 to select +3.3VD as the source for the digital buffer voltage supply (+BVDD).

Table 4-2. Power Connector, J1, Pinout

Signal	Power Connector - J1		Signal
+VA(+7V)	1	2	–VA (–7V)
+5VA	3	4	N/C
DGND	5	6	AGND
N/C	7	8	N/C
+3.3VD	9	10	+5VD

Chapter 5

Using the EVM

The ADS8402/ADS8412EVM serves three functions:

1) As a reference design
2) As a prototype board
3) As a software test platform

Topic **Page**

5.1 As a Reference Board

As a reference design, the ADS8402/ADS8412EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The EVM analog input circuit is optimized for 100-kHz sine wave. Therefore, users may need to adjust the resistor and capacitor values of the A/D input circuit. In ac-type applications where signal distortion is a concern, polypropylene capacitors should be used in the signal path.

5.2 As a Prototype Board

As a prototype board, the buffer circuit consists of resistor pads for configuring the input as either single-ended or differential input. The input circuit can be modified to accommodate user prototype needs, whether it be evaluating another differential amplifier or limiting noise for best performance. The analog, power, and digital connectors can be made to plug into a standard 0.1 in. breadboard or cables made up to interface directly to an FPGA or processor.

5.3 As a Software Test Platform

As a software test platform, connectors P1, P2, and P3, plug into the parallel interface connectors of the 5-6K interface card. The 5-6K interface card sits on the C5000 and C6000 digital signal processor starter kit (DSK). The ADS8402/ADS8412EVM is then mapped into the processor's memory space. This card also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8402/ADS8412 analog-to-digital converter. See the 5-6K interface card user's guide (SLAU104) for more information.

The ADS8402/ADS8412EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-in. headers and sockets to wire into prototype boards. The user only needs to provide three address lines (A2, A1, A0) and address valid line ($\overline{\text{DC_CS}}$) to connector P2. To choose which address combinations generates $\overline{\text{RD}}$, $\overline{\text{CONVST}}$, and $\overline{\text{RESET}}$, set jumpers as shown in Table 4-2. The recall chip select ($\overline{\text{CS}}$) signal is not memory-mapped or tied to P2; therefore, it must be controlled via a general purpose pin or shorted to ground at J3 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus via P3 and control via J3.

Chapter 6

ADS8402/ADS8412EVM BOM, Layout, and Schematic

This chapter contains the ADS8402/ADS8412EVM bill of materials, the layouts, and the schematics.

Topic **Page**

6.1 ADS9393EVM Bill of Materials

Table 6-1 contains a complete bill of materials for the ADS8402/ADS8412EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail dataconvapps@list.ti.com for questions regarding this EVM.

Table 6-1. ADS8402/ADS8412EVM Bill Of Materials

Item No.	QTY	Value	Designator	Footprint	Mfg	Mfg's Part Number	Description
1	2	0 Ω	R15, R21	805	Panasonic - ECG or Alternate	ERJ-6GEY0R00V	RES 0 Ω 1/8 W 5% 0805 SMD
2	2	24.9 Ω	R12, R13	805	Panasonic - ECG or Alternate	ERJ-6ENF24R9V	RES 24.9 Ω 1/10 W 1% 0805 SMD
3	3	100 Ω	R5, R14, R25	805	Panasonic - ECG or Alternate	ERJ-6ENF1000V	RES 100 Ω 1/10 W 1% 0805 SMD
4	1	910 Ω	R4	805	Panasonic - ECG or Alternate	ERJ-6GEYJ911V	RES 910 Ω 1/8 W 5% 0805 SMD
5	3	1 kΩ	R1, R7, R10	805	Panasonic - ECG or Alternate	ERJ-6ENF1001V	RES 1 kΩ 1/10 W 1% 0805 SMD
6	5	10 kΩ	R16 - R20	603	Panasonic - ECG or Alternate	ERJ-3EKF1002V	RES 10 kΩ 1/16 W 1% 0603 SMD
7	1	10 kΩ	R24	805	Panasonic - ECG or Alternate	ERJ-6ENF1002V	RES 10 kΩ 1/10 W 1% 0805 SMD
8	6	NI	R6, R8, R11, R2, R3, R22	805	Not Installed	Not Installed	
9	1	49.9 Ω	R23	805	Panasonic - ECG or Alternate	ERJ-6ENF49R9V	RES 49.9 Ω 1/10 W 1% 0805 SMD
10	4	1 nF	C3, C5, C11, C23	1206	Kemet or Alternate	C1206C102J5GACTU	Capacitor 1000 pF 50-V ceramic NPO 1206
11	2	68 pF	C34, C35	TH	WIMA	FKP2 68/100/1	68-pF polypropylene capacitor
12	1	6800 pF	C17	TH	WIMA	FKP2 6800/100/1	6800-pF polypropylene capacitor
13	10	0.01 μF	C13, C21, C41, C44, C46, C48, C53, C56, C65, C50	603	Kemet or Alternate	C0603C103J5RACTU	Capacitor 10000 pF 50-V ceramic X7R 0603
14	4	0.01 μF	C10, C18, C20, C66	805	Kemet or Alternate	C0805C103K5RACTU	Capacitor 10000 pF 50-V ceramic X7R 0805
15	2	0.01 μF	C4, C26	1206	Kemet or Alternate	C1206C103J5RACTU	Capacitor 10000 pF 50-V ceramic X7R 1206
16	15	0.1 μF	C8, C25, C40, C42, C43, C47, C51, C52, C54, C55, C57, C58, C62, C63, C64	603	Kemet or Alternate	C0603C104K3RACTU	Capacitor 0.1 μF 25-V ceramic X7R 0603
17	7	0.1 μF	C7, C9, C15, C22, C32, C36, C45	805	Kemet or Alternate	C0805C104J5RACTU	Capacitor 0.10 μF 50-V ceramic X7R 0805
18	6	1 μF	C16, C31, C33, C37, C59, C60	805	Kemet or Alternate	C0805C105K4RACTU	Capacitor 1 μF 16-V ceramic X7R 0805
19	2	1 μF	C2, C28	1206	Kemet or Alternate	C1206C105K3RACTU	Capacitor 1 μF 25-V ceramic X7R 1206
20	4	10 μF	C1, C6, C12, C19	1206	Panasonic - ECG or Alternate	ECJ-3YB1C106M	Capacitor 10 μF 16-V ceramic X5R 1206
21	1	10 μF	C49	3528	Kemet or Alternate	T491B106K016AS	Capacitor TANT 10 μF 16 V 10% SMT

Item No.	QTY	Value	Designator	Footprint	Mfg	Mfg’s Part Number	Description
22	4	10 μF	C14, C24, C27, C29	6032	Panasonic - ECG or Alternate	ECS-T1EC106R	Capacitor 10 μF 25-V tantalum TE SMD
23	1	22 μF	C30	805	TDK Corporation	C2012X5R0J226M	Capacitor CER 22 μF 6.3 V X5R 20% 0805
24	3	NI	C38, C39, C61	805			
25	2	1 Ω	RP1, RP3	CTS_742	CTS Corporation	742C163102JTR	RES array 1 Ω 16TERM 8RES SMD
26	1	100 Ω	RP2	CTS_742	CTS Corporation	742C163101JTR	RES array 100 Ω 16TRM 8RES SMD
27	1	10 kΩ	R9	BOURNS_32X4W	Bourns	3214W-1-103E	TRIMPOT 10 kΩ 4 mm top ADJ SMD
28	4		L1, L2, L3	1206	MURATA ERIE	BLM31PG601SN1L	Chip ferrite beads- 600 Ω at 100 MHz
29	2		U1, U3	3-SOT-23	Texas Instruments	REF3040AIDBZT	REF3040 50 ppm/°C, 50 μA in SOT23-3 CMOS voltage reference
30	1		U2	8-SOP(D)	Texas Instruments	THS4503ID	High-speed fully-differential amplifiers
31†	1		U4	socket_48QFP	Texas Instruments	ADS8402IPFBT†	ADS8402 16-bit 1.25 MSPS
32	1	OPA627AU	U8	8-SOP(D)	Not installed	Not installed	Amplifier
33	1	NI	U9	8-SOP(D)			Footprint for 8-pin SOIC reference that operates from +5V.
34	1		U10	5-SOT (DBV)	Texas Instruments	SN74AHC1G04DBVR	Single inverter gate
35	1		U11	16-TSSOP (PW)	Texas Instruments	SN74AHC138PWR	3-line to 8-line decoder / demultiplexer
36	3		U5, U6, U7	20-TSSOP (PW)	Texas Instruments	SN74AHC245PWR	Octal bus transceiver, tri state
37	1	5X2X.1	J1	5X2X.1_SMT_socket	Samtec	TSM-105-01-T-D-V-P	0.025” SMT plug - top side of PWB
38	1	6X2X.1	J3	6X2X.1_SMT_plug_&_socket	Samtec	SSW-106-22-S-D-VS	0.025” SMT socket - bottom side of PWB
						TSM-106-01-T-D-V-P	0.025” SMT plug - top side of PWB
39	2	SMA_PCB_MT	J2, J4	SMA_JACK	AMPHENOL	901-144-4	MaCom #5002-5003-10 / Amphenol #901-144
40	2	10X2X.1	P1, P2	10X2X.1_SMT_plug_&_socket	Samtec	SSW-110-22-S-D-VS	0.025” SMT socket - bottom side of PWB
						TSM-110-01-T-D-V-P	0.025” SMT plug - top side of PWB
41	1	16X2X.1_SMT_plug_&_socket	P3	16X2X.1_SMT_plug_&_socket	Samtec	SSW-116-22-S-D-VS	0.025” SMT socket – bottom side of PWB
						TSM-116-01-T-D-V-P	0.025” SMT plug – top side of PWB
42	1	SJP2	SJP3	SJP2	Not installed	Not installed	Pad 2 position jumper
43	3	SJP3	SJP2, SJP4, SJP5	SJP3	Not installed	Not installed	Pad 3 postion jumper
44	1	SW-PB	S1	EVQ-PJ	Panasonic	EVQ-PJU04K	Switch
45	5	3POS_JUMPER	W1 - W5	3pos_jump	Samtec	TSW-103-07-L-S	3 position jumper 0.1” spacing
46	14	TP_.025	TP1 - TP14	test_point2	Keystone Electronics	5000K–ND	Test point-single 0.025” pin

Note: On ADS8412EVM, the ADS8412IPFBT is installed instead of ADS8402IPFBT.

6.2 ADS8402/ADS8412EVM Layout

Figure 6-1. Top Layer—Layer 1

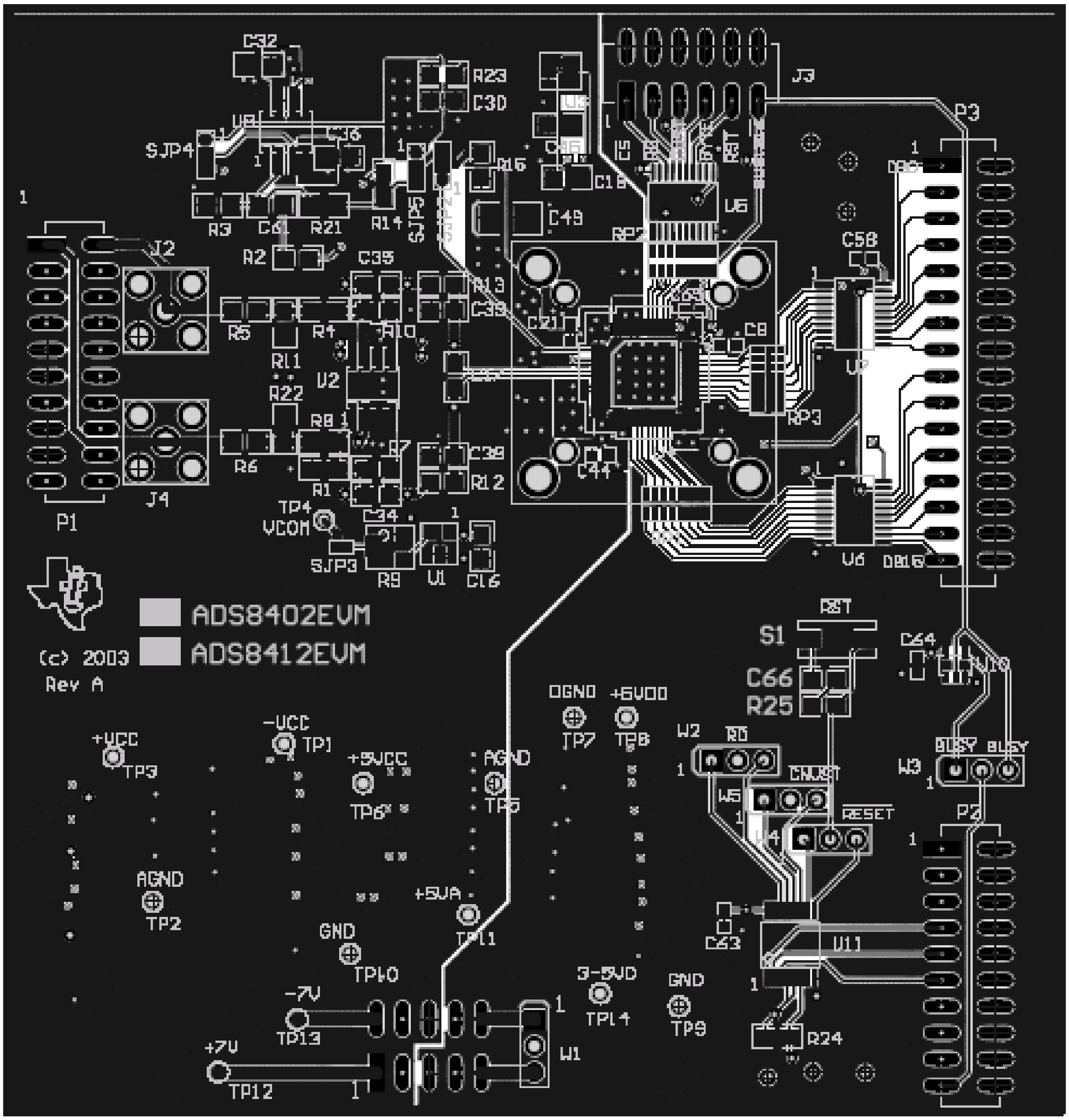


Figure 6-2. Ground Plane—Layer 2

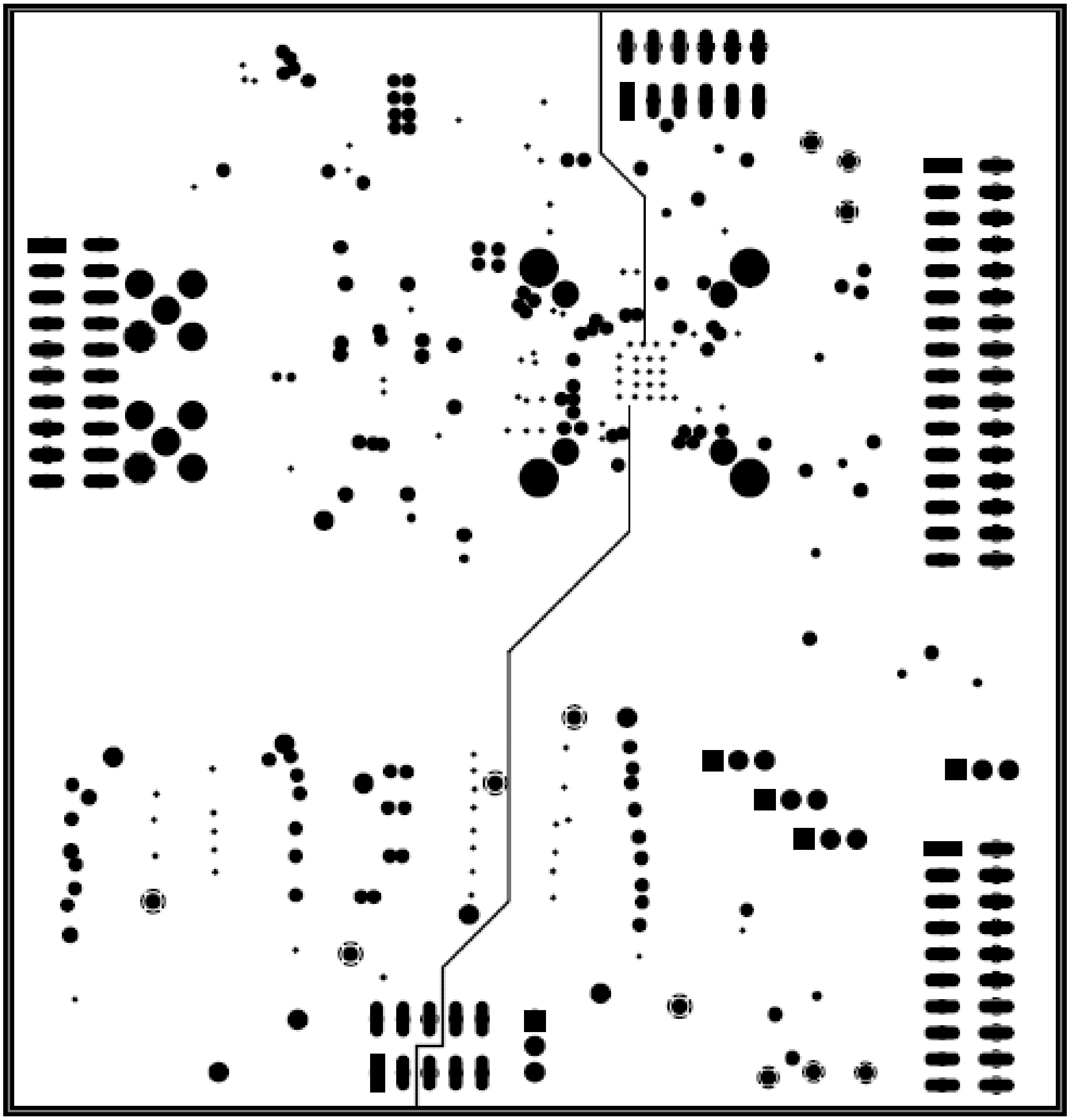


Figure 6-3. Power Plane—Layer 3

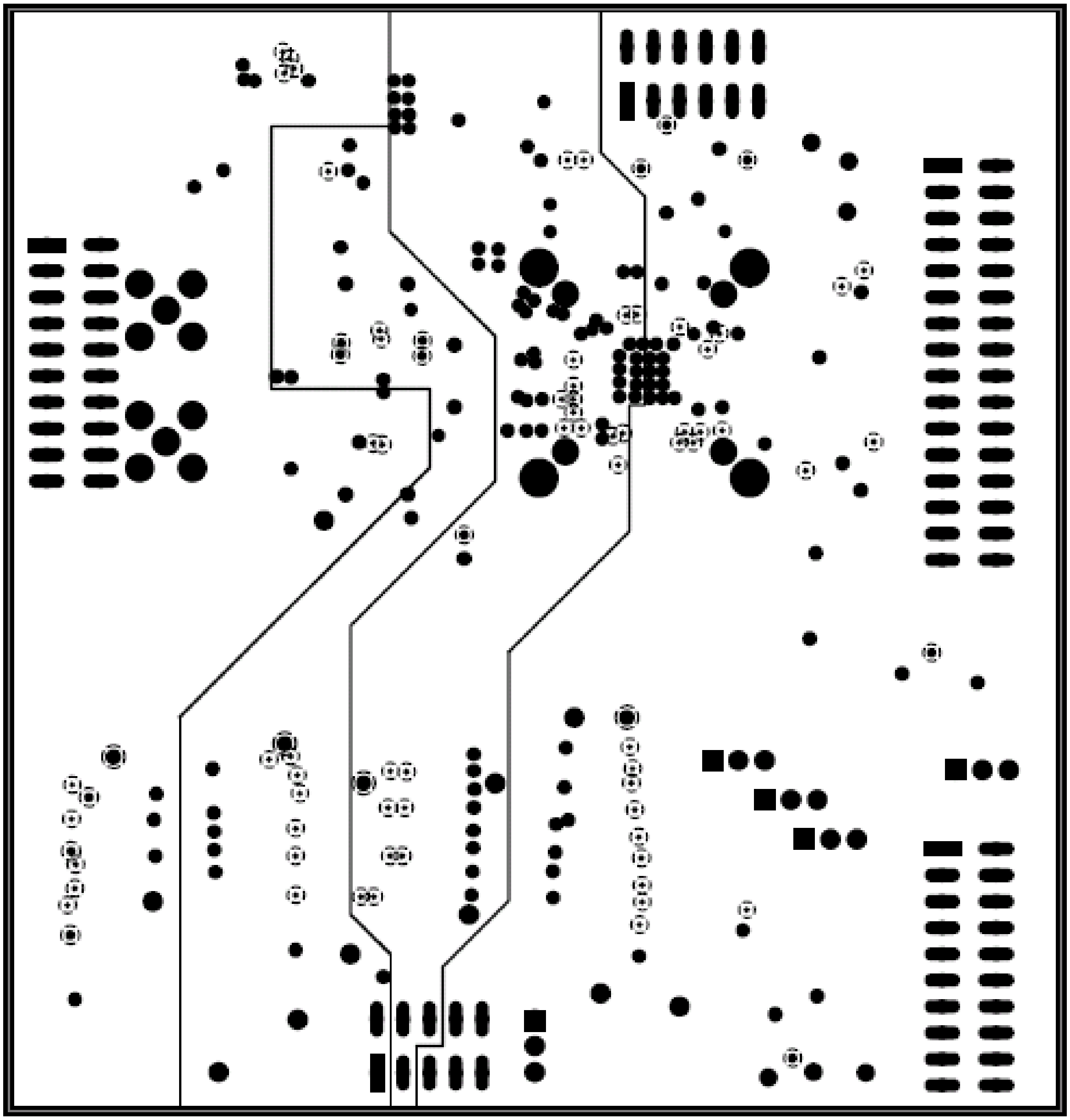
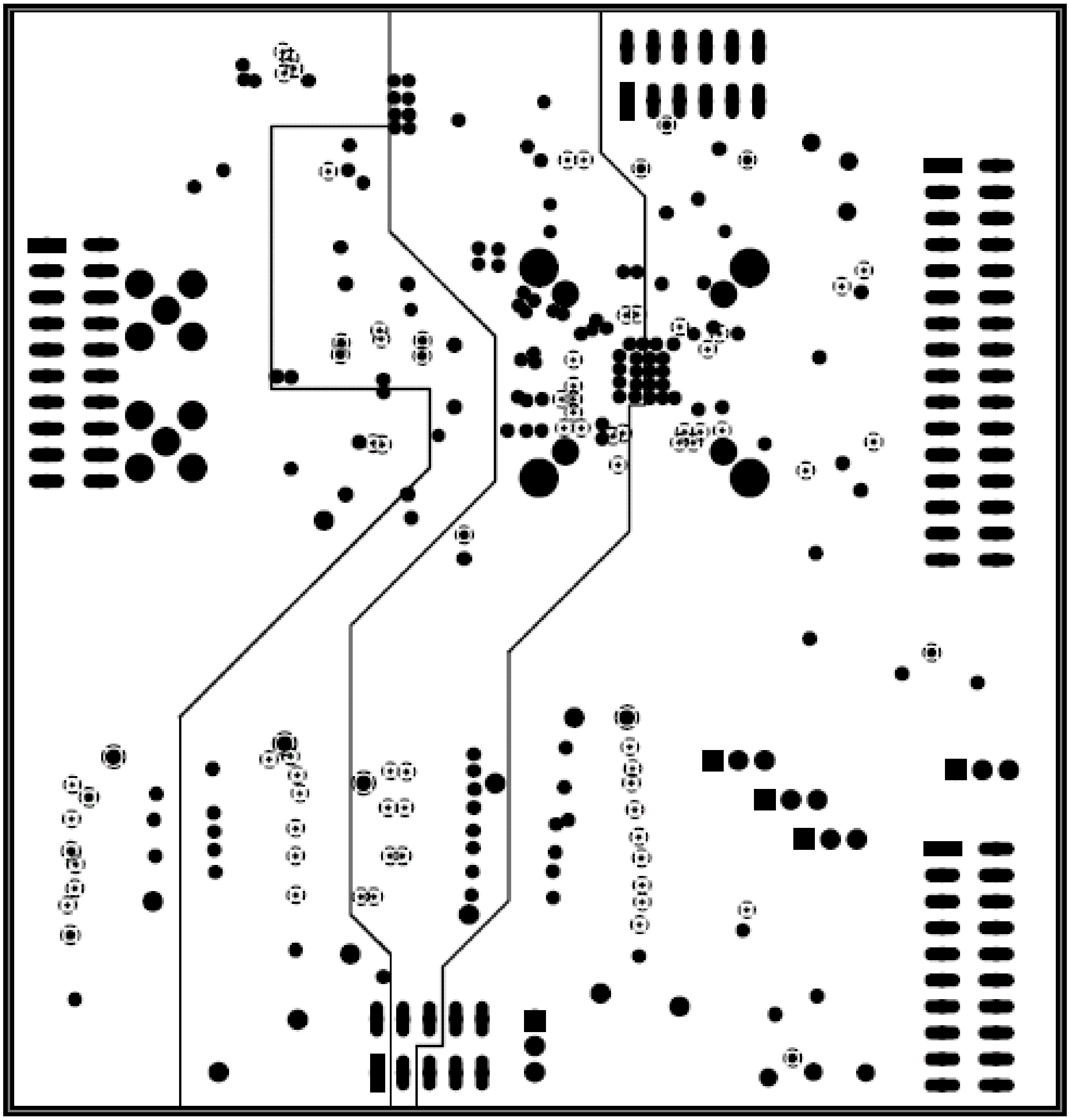
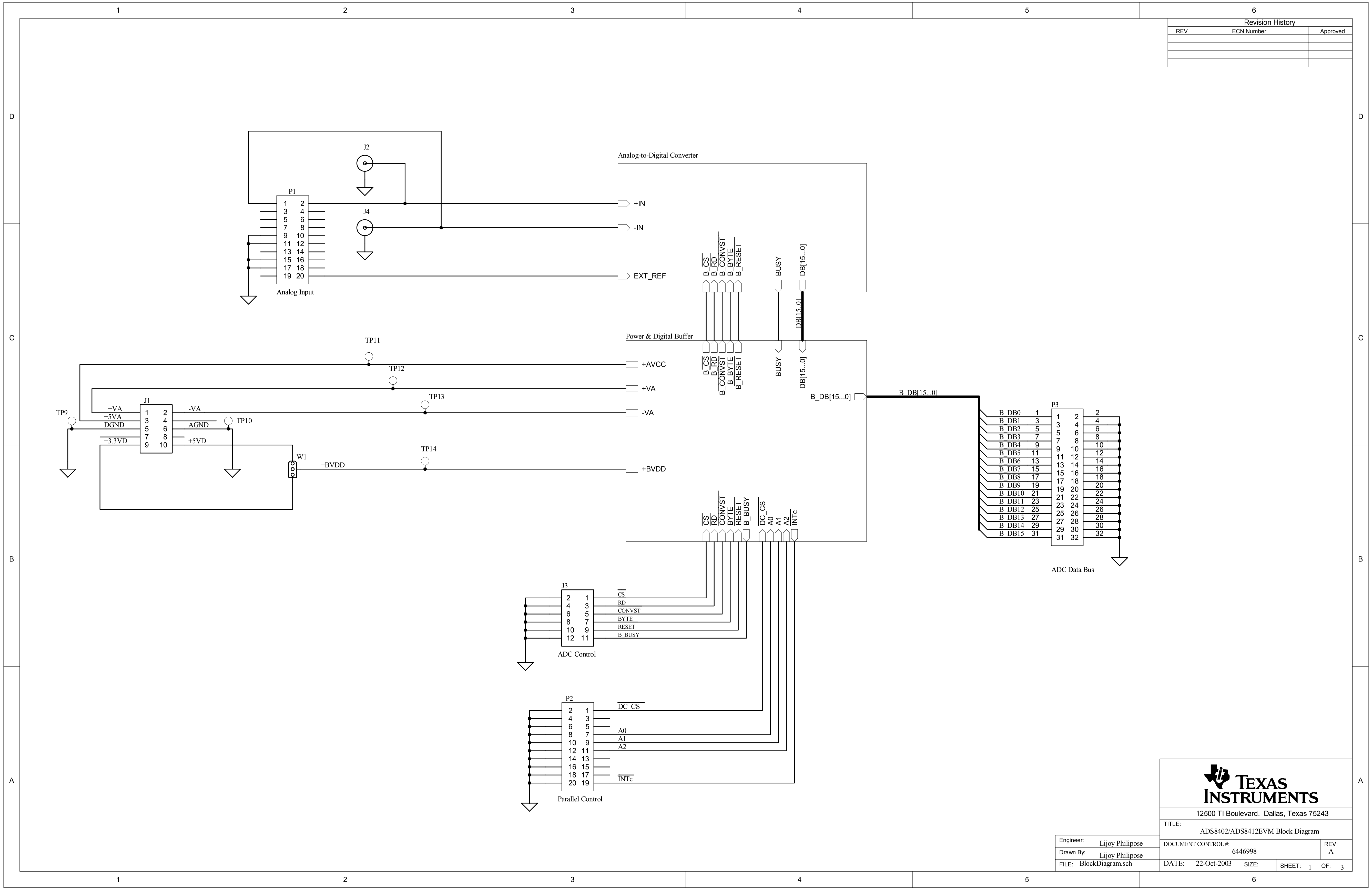


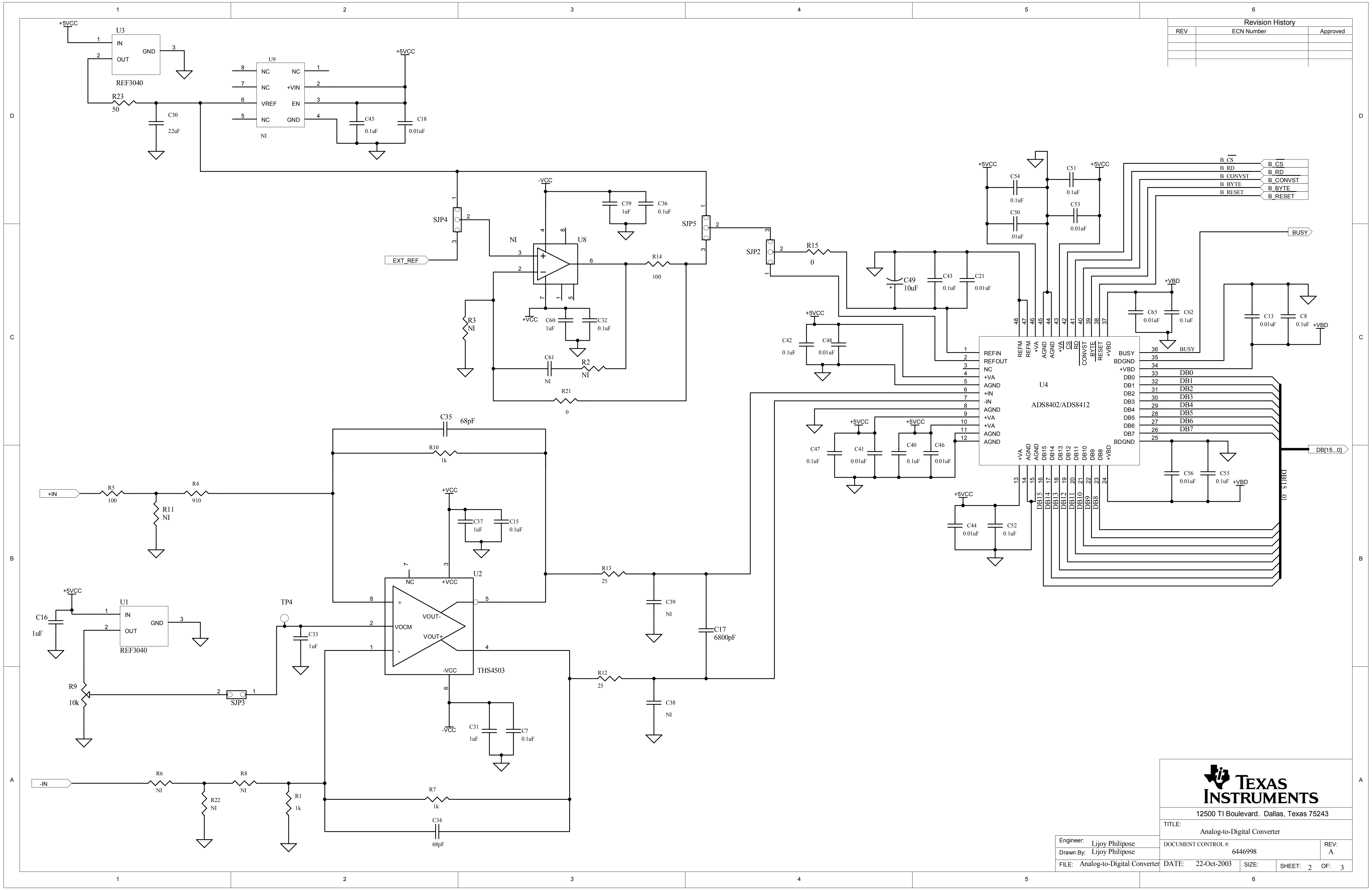
Figure 6-4. Bottom Layer—Layer 4

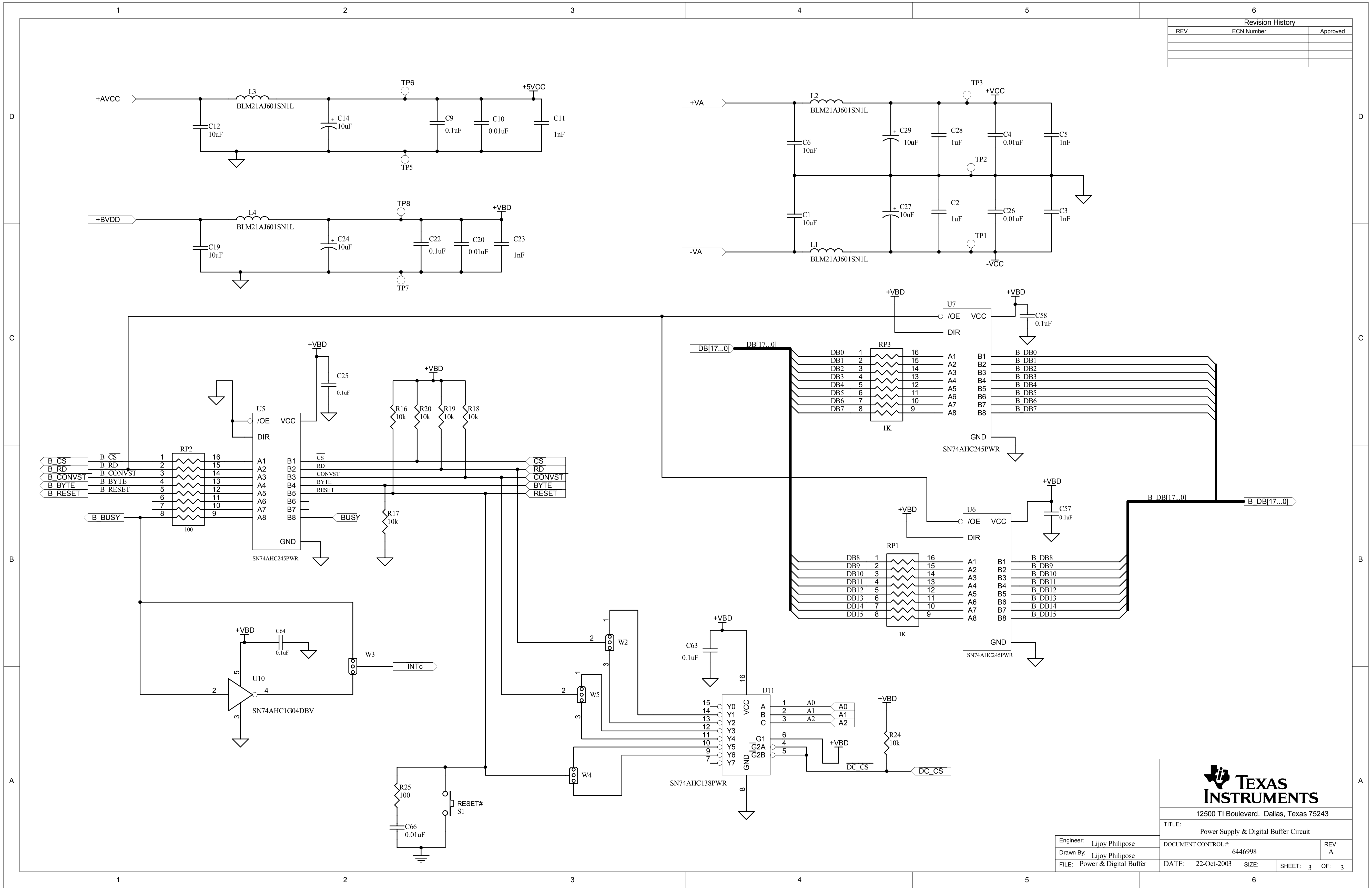


6.3 ADS8402/ADS8412EVM Schematic

The following pages contain the schematic for the ADS8402/ADS8412EVM.


Revision History
REV
ECN Number
Approved
Analog-to-Digital Converter
Power & Digital Buffer
P1
Analog Input
J2
J4
+IN
-IN
EXT_REF
B_CS
B_RD
B_CONVST
B_BYTE
B_RESET
BUSY
DB[15...0]
+AVCC
+VA
-VA
+BVDD
B_DB[15...0]
TP9
TP10
TP11
TP12
TP13
TP14
J1
+5VA
DGND
AGND
+3.3VD
+5VD
W1
CS
RD
CONVST
BYTE
RESET
B_BUSY
DC_CS
A0
A1
A2
INTc
J3
ADC Control
P2
Parallel Control
P3
B_DB0
B_DB1
B_DB2
B_DB3
B_DB4
B_DB5
B_DB6
B_DB7
B_DB8
B_DB9
B_DB10
B_DB11
B_DB12
B_DB13
B_DB14
B_DB15
ADC Data Bus
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE: ADS8402/ADS8412EVM Block Diagram
Engineer: Lijoy Philipose
Drawn By: Lijoy Philipose
FILE: BlockDiagram.sch
DOCUMENT CONTROL #: 6446998
REV: A
DATE: 22-Oct-2003
SIZE:
SHEET: 1 OF: 3


Revision History
REV
ECN Number
Approved
U3
REF3040
U9
U8
U2
THS4503
U1
U4
ADS8402/ADS8412
12500 TI Boulevard. Dallas, Texas 75243
TITLE: Analog-to-Digital Converter
Engineer: Lijoy Philipose
Drawn By: Lijoy Philipose
FILE: Analog-to-Digital Converter
DOCUMENT CONTROL #: 6446998
REV: A
DATE: 22-Oct-2003
SIZE:
SHEET: 2 OF: 3



Revision History
REV
ECN Number
Approved
+AVCC
L3
BLM21AJ601SN1L
TP6
+5VCC
C12 10uF
C14 10uF
C9 0.1uF
C10 0.01uF
C11 1nF
TP5
+BVDD
L4
BLM21AJ601SN1L
TP8
+VBD
C19 10uF
C24 10uF
C22 0.1uF
C20 0.01uF
C23 1nF
TP7
+VA
L2
BLM21AJ601SN1L
TP3
+VCC
C6 10uF
C29 10uF
C28 1uF
C4 0.01uF
C5 1nF
TP2
C1 10uF
C27 10uF
C2 1uF
C26 0.01uF
C3 1nF
TP1
-VA
L1
BLM21AJ601SN1L
-VCC
U7
SN74AHC245PWR
C58 0.1uF
DB[17...0]
RP3
1K
U6
SN74AHC245PWR
C57 0.1uF
RP1
1K
B_DB[17...0]
U5
SN74AHC245PWR
C25 0.1uF
RP2
100
R16 10k
R20 10k
R19 10k
R18 10k
R17 10k
B_CS
B_RD
B_CONVST
B_BYTE
B_RESET
B_BUSY
CS
RD
CONVST
BYTE
RESET
BUSY
U10
SN74AHC1G04DBV
C64 0.1uF
W3
INTc
W2
W5
W4
C63 0.1uF
U11
SN74AHC138PWR
A0
A1
A2
R24 10k
DC_CS
R25 100
C66 0.01uF
RESET#
S1
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE: Power Supply & Digital Buffer Circuit
Engineer: Lijoy Philipose
Drawn By: Lijoy Philipose
FILE: Power & Digital Buffer
DOCUMENT CONTROL #: 6446998
REV: A
DATE: 22-Oct-2003
SIZE:
SHEET: 3 OF: 3